CLAIMS

What is claimed is:

1. A method for carrying out failure analysis of integrated circuit semiconductor device conductive portions comprising the steps of:

providing an integrated circuit (IC) semiconductor device comprising at least one conductive interconnect portion;

providing a printed circuit board (PCB) comprising a current signal amplification circuit having a current signal input side and a current signal output side for outputting an amplified current signal;

mounting the IC semiconductor device such that the at least one conductive interconnect portion is electrically connected between a ground potential of the PCB and the current signal input side;

mounting the PCB comprising the IC semiconductor device in a scanning electron microscope (SEM) for impacting a surface of the IC semiconductor device with a primary electron beam;

exposing at least a portion of the IC semiconductor device to the primary electron beam to induce a current signal within the conductive portions;

passing the current signal through the amplification electronics to amplify the current signal; and,

outputting the amplified current signal from the current signal output side to an image display system input side to produce an image comprising a brightness contrast.

2. The method of claim 1, wherein the PCB comprises a pre-amplifier board (PAB) including a current signal amplification circuit having at least one CMOS differential amplifier.

3. The method of claim 2, wherein the at least one CMOS differential amplifier comprise one of single and multistage CMOS operational amplifiers.

4. The method of claim 1, wherein the current signal is amplified by at least about a factor of 10^6.

5. The method of claim 1, wherein the current signal is sampled at a bandwidth of greater than about 400 kHz.

6. The method of claim 2, wherein the at least one CMOS differential amplifier is DC biased at from about minus 20 Volts to about plus 20 Volts.

7. The method of claim 1, wherein the primary electron beam is adjusted to have an accelerating voltage from about 100 eV to about 10000 eV.

8. The method of claim 1, wherein the primary electron beam is adjusted to have an accelerating voltage of less than about 3000 eV.

9. The method of claim 1, wherein the IC semiconductor device comprises multi-level metallization layers.

10. The method of claim 9, wherein the surface of the IC semiconductor device comprises an exposed surface of the at least one conductive interconnect.

11. The method of claim 10, wherein the surface of the IC semiconductor device comprises at least one passivation layer overlying the at least one conductive interconnect.

12. The method of claim 1, wherein a second current signal produced by detection of secondary electrons emitted from the IC semiconductor device is convoluted with the current signal to produce a composite image.

13. A method for carrying out failure analysis of integrated circuit semiconductor device conductive portions comprising the steps of:

provideing an integrated circuit (IC) semiconductor device comprising conductive portions;

providing a pre-amplifier board (PAB) comprising current signal amplification electronics having a current signal input side and a current signal output side for outputting an amplified current signal;

mounting the IC semiconductor device in electrical communication with ground potential of the PAB and the current signal input side;

mounting the PAB comprising the IC semiconductor device on a moveable stage in a scanning electron microscope (SEM) for probing the IC semiconductor device with a primary electron beam;

exposing at least a portion of the IC semiconductor device to the primary electron beam to induce a current signal within the conductive portions;

amplifying the current signal by a factor of about 10^6 at a bandwidth of greater than about 400 kHz; and,

outputting the amplified current signal to an image display system to produce an image representative of an electrical resistance of the conductive portions.

14. The method of claim 13, wherein the PAB comprises at least one CMOS differential amplifier.

15. The method of claim 14, wherein the at least one CMOS differential amplifier is DC biased at from about minus 20 Volts to about plus 20 Volts.

16. The method of claim 13, wherein the primary electron beam is adjusted to have an accelerating voltage of less than about 3000 eV.

17. The method of claim 13, wherein the IC semiconductor device comprises multi-level metallization layers.

18.   The method of claim 17, wherein the surface of the IC semiconductor device comprises an exposed surface of the at least one conductive interconnect.

19.   The method of claim 17, wherein the surface of the IC semiconductor device comprises at least one passivation layer overlying the at least one conductive interconnect.

20.   The method of claim 13, wherein a second current signal produced by detection of secondary electrons emitted from the IC semiconductor device is convoluted with the current signal to produce a composite image.

21.   An SEM in-situ sample amplification system for carrying out in-situ current amplification of electron beam induced current to increase a current detection sensitivity comprising:

a printed circuit board (PCB) comprising a current signal amplification circuit said current signal amplification circuit comprising a current signal input side and a current signal output side for outputting an amplified current signal;

an IC semiconductor device mounted on the PCB adjacent the current signal input side said IC semiconductor device comprising a conductive interconnect pathway disposed in electrical

communication with the PCB ground potential and the current

signal input side;

wherein the PCB comprising the IC semiconductor device is

mountable in a scanning electron microscope (SEM) for probing the

IC semiconductor device with a primary electron beam to produce

the amplified current signal for input to an input side of an

image display unit.

22. The SEM in-situ sample amplification system of claim 21,

wherein the current signal amplification circuit comprises a pre-

amplifier board (PAB) including at least one CMOS differential

amplifier.

23. The SEM in-situ sample amplification system of claim 22,

wherein the at least one CMOS differential amplifier comprises

NMOS and PMOS transistors connected in series.

24. The SEM in-situ sample amplification system of claim 21,

wherein the PCB comprises an electrically insulating polymeric

material.

25.   The SEM in-situ sample amplification system of claim 21,

wherein the current signal amplification circuit is capable of

amplifying the current signal by at least about a factor of 10^6.

26.   The SEM in-situ sample amplification system of claim 21,

wherein the current signal is detectable to a level of about 1

pico-ampere.

27.   The SEM in-situ sample amplification system of claim 21,

wherein the current signal amplification circuit operates at a

signal bandwidth of greater than about 400 kHz.

28.   The SEM in-situ sample amplification system of claim 21,

wherein the PCB further comprises a DC power source for biasing

the at least one differential amplifier from about minus 20

Volts to about plus 20 Volts.

29.   The SEM in-situ sample amplification system of claim 21,

wherein the IC semiconductor device comprises multi-level

metallization layers comprising conductive interconnects.

30.   The SEM in-situ sample amplification system of claim 21,
wherein the surface of the IC semiconductor device comprises an
exposed surface of the conductive interconnects.

31.   The SEM in-situ sample amplification system of claim 21,
wherein the surface of the IC semiconductor device comprises at
least one passivation layer disposed over the conductive
interconnects.